Suleiman *Abu Kharmeh*
suleiman@abukharmeh.com
T: +44 (0) 207 1934509

3rd floor, 207 regent street
London, W1B 3HH
United Kingdom

Objective and Profile

Suleiman Abu Kharmeh is a digital design and verification contractor who has recently worked on projects with NXP Semiconductors Germany GmbH in Hamburg, Renesas Electronics Europe GmbH in Dusseldorf, Intel Mobile Communications Group in Dresden and STMicroelectronics in Grenoble. In those projects, the focus was on the integration and verification of designs at the subsystem/IP level. Between contracts, he enjoys his research work in the field of formal hardware design and complexity analysis as well as lecturing in Computer Architecture and Logic Design.

Professional Background Highlights

- NXP Semiconductors Germany GmbH — Hamburg, Germany
  Digital Design Engineering Consultant — *July 2016 - to-date*
  - Post-silicon validation SW/HW setup: drivers, monitors and software APIs.
  - Analysis and debugging using oscilloscope, source meter and DMM.

- Renesas Electronics Europe GmbH — Dusseldorf, Germany
  Hardware Design and Verification Consultant — *Jan. 2016 - June 2016*
  - Setting up mixed **SystemVerilog** environments (**VMM** and **UVM**).
  - Specification and implementation of testbench architecture (generators, drivers, monitors and checkers/scoreboards).
  - Integration of **VMM Verification IP** into the verification flow.
  - Implementation of test cases, assertions and covergroups (pseudo-random and directed).
  - Monitoring regression and coverage results using **VCS** and **DVE**.

- Intel Mobile and Communications GmbH — Dresden, Germany
  Hardware Design and Verification Consultant — *Jun. 2014 - Nov. 2014*
  - Implementation, integration and verification of requirements in **VHDL**, **IP-XACT** and **UPF**.
  - Setting up **environment for power aware verification** using **XML**, **Java** and **Make**.
  - Defining, implementing and monitoring **low power coverage plan** using **SystemVerilog**, **TCL**, **VCS-NLP** and **DVE**.

- ST Microelectronics — Grenoble, France
  Hardware Verification Consultant — *Aug. 2012 - Dec. 2012*
  - Specification of power aware verification test-plan at IP integration/subsystem level of **GPU**.
  - Implementation of verification API using **C, Verilog and SystemVerilog**.
  - **2D/3D GPU** verification using **Synopsys** functional and low-power simulators (**VCS** and **MVSIM/NLP**).

Skills

- **Technical Skills**
  - Hardware Design and Implementation: **VHDL, Verilog, SystemVerilog**, **UPF** and **IP-XACT**.
  - Verification and Model-Checking methodologies and tools: **UVM, VCS, MVSIM/NLP, ModelSim, Quartus**.
  - Microcontrollers: **Intel 8086 family, Altera NiosII, XMOS XCore and Microchip PIC**.
  - Other Languages: **Compilers, code generators**, **C++**, Assembly languages, Java, .
  - Scripting Languages: Shell programming, **TCL** and **Make**.
  - Revision Control: **ClearCase**, **SVN** and CVS.
  - Operating Systems: **Linux** and Windows.
- **Core Skills**
  - **Target Driven:** Determined and attentive to details while keeping the target in sight.
  - **Calm and Collected:** Able to work efficiently under pressure.
  - **Effective Communicator:** Competent in both verbal and written communications.
  - **Enthusiastic,** Positive and optimistic at all times.

Academic Background

- PhD, University of Bristol — Bristol, UK
  Microelectronics and Computer Engineering — *Jan. 2008 - Sep. 2013*
  - Thesis date: Aug. 2012
  - Thesis title: Formal Complexity-Oriented Performance-Critical Design and Verification Framework.
- MSc with Distinction, University of Bristol — Bristol, UK
  Advanced Microelectronics Systems Engineering — *Oct. 2006 - Sep. 2007*
  - Dissertation: Research and Implementation of Security Requirements of the XCore processor.
  - Selected Subjects: **Advanced Computer Architecture, Design Verification, System Integration, Digital System, Embedded Real Time Systems and Advanced Language Engineering**.
- An-Najah National University — Nablus, Palestine
  Bachelor of Computer Engineering — *Sep. 2000 - Dec. 2005*
  - Final GPA: High Good (86.5%)

Technical Training

- Doulos Training Centre — Ringwood, UK
  Universal Verification Methodology (UVM) Adopter Class — *Sep. 2015*
  - Training in advanced **SystemVerilog** methodologies using UVM
  - Topics covered include: Functional Coverage, Random Stimulus Generation and UVM Code Generator

Publications

[1] Suleiman Abu Kharmeh. *Formal Complexity-Oriented Performance-Critical Design and Verification Framework*. PhD thesis, University of Bristol, 2012.

[2] Suleiman Abu Kharmeh, Kerstin Eder, and David May. A Design-for-Verification Framework for a Configurable Performance-Critical Communication Interface. In *Proc. 9th Int. Conf. Formal Modeling and Anal. of Timed Syst.*, pages 335–351. Springer, August 2011.

[3] Suleiman Abu Kharmeh, Kerstin Eder, and David May. Formal Analysis of a Programmable Performance-Critical Processor Communication Interface. In *Proc. 10th AVoCS Int. Workshop*, 2010.

[4] Suleiman Abu Kharmeh and Simon Hollis. Reconfigurable High-speed Asynchronous I/O Ports for Flexible Protocol Support. In *Proc. 20th UK Asynchronous Forum*, 2008.

[5] Suleiman Abu Kharmeh. Research and Implementation of Security Requirements of the XCore Processor. Master's thesis, University of Bristol, 2007.

[6] Andrew Lynch, Suleiman Abu Kharmeh, John Barton, Brendan O'Flynn, Philip Angove, and S C O Mathuna. Design and characterisation of a wireless inertial measurement unit for integration to a wireless network scenario. In *Proc. Information Technology and Telecommunications Conf.*, pages 245–247, Cork Institute of Technology, Ireland, 2005.

Seminars

[1] Suleiman Abu Kharmeh. A Design-for-Verification approach of a Configurable Performance-Critical Concurrent Communication Interface. Department of Computer Science, University of Oxford, February 2011.

Hobbies & Activities

- **Swimming, Weights, Cycling and Rowing**